REMARKS/ARGUMENTS

Applicants received the final Office action dated July 15, 2004, in which the Examiner: (1) rejected claims 1-4, 9-12, 17-19, 24-28 and 33-35 as anticipated by "Compiler Optimizations for Improving Data Locality," 1994, ACM, pages 252-262 (hereinafter referred to as the "Carr" reference); and (2) rejected claims 5-8, 13-16, 20-23 and 29-32 as obvious in view of Carr and U.S. Patent No. 5,797,013 ("Mahadevan"). In this Response, Applicants amend the specification and claims 1, 9, 17, 24-26, 33 and 35. Also, Applicants add claims 36-40. Based on the arguments and amendments contained herein, Applicants believe all claims to be in condition for allowance. Accordingly, Applicants respectfully request reconsideration and allowance of the pending claims.

I. § 102 AND § 103 REJECTIONS

A. Claim 1

Amended claim 1, in part, requires "distributing the vector memory references into a plurality of detail loops configured to allocate the vector memory references into a plurality of temporary arrays, sized and located, so that none of the vector memory references are cache synonyms." Carr does not teach or suggest this limitation.

Carr teaches "loop distribution" that "separates independent statements in a single loop into multiple loops with identical headers" (see pg. 256, section 4.4 and Figure 5). However, Carr does not teach or suggest "detail loops configured to allocate the vector memory references into a plurality of temporary arrays, sized and located, so that none of the vector memory references are cache synonyms" as required in claim 1.

Further, Carr must be considered in its entirety, including disclosures that teach away from the claims (MPEP 2143.02). Specifically, Carr teaches a system that "only use[s] loop distribution to indirectly improve reuse by enabling loop permutation on a nest that is not permutable" (see pg. 256, section 4.4). The distribution algorithm implemented by Carr is only called "if memory order cannot be achieved on a nest and not all the inner nests can be fused" (see pg. 256, section 4.4). In other words, Carr teaches using loop distribution for a specified purpose that is different from the recitations of claim 1.

Carr does suggest "distribution could also be effective if there is no temporal locality between partitions and the accessed arrays are too numerous to fit in cache at once," however, Carr specifically states that this issue in not addressed (see Footnote 3). Carr does not provide any additionally information regarding the use of distribution and does not teach or suggest "distributing the vector memory references into a plurality of detail loops configured to allocate the vector memory references into a plurality of temporary arrays, sized and located, so that none of the vector memory references are cache synonyms" as required in claim 1.

The Examiner cannot argue that distribution inherently teaches the claimed invention without providing rationale or evidence tending to show inherency (MPEP 2112). The fact that a certain result or characteristic may occur or be present is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531. Neither the text nor the distribution algorithm of Carr teaches or suggests "distributing the vector memory references into a plurality of detail loops configured to allocate the vector memory references into a plurality of temporary arrays, sized and located, so that none of the vector memory references are cache synonyms" as required in claim 1. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 1 and all claims that depend from claim 1 are allowable.

B. Claim 9

Amended claim 9, in part, requires "distributing the vector memory references into a plurality of detail loops that serially proceed through strips of the vector memory references and store the strips in temporary arrays so that none of the vector memory references are cache synonyms." Carr does not teach or suggest this limitation.

As previously described, Carr must be considered in its entirety, including disclosures that teach away from the claims. Further, the Examiner cannot argue that distribution inherently teaches the claimed invention without providing rationale or evidence tending to show inherency. Neither the text nor the distribution algorithm of Carr teaches or suggests "detail loops that serially

proceed through strips of the vector memory references and store the strips in temporary arrays so that none of the vector memory references are cache synonyms" as required in claim 9. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 9 and all claims that depend from claim 9 are allowable.

C. Claim 17

Amended claim 17, in part, requires "distributing the vector memory references into a plurality of detail loops in response to cache behavior and the dependencies between the vector memory references in the loop." Claim 17 further requires "the detail loops cause storage of the vector memory references in temporary arrays that are allocated consecutively so that no temporary arrays elements are cache synonyms." Carr does not teach or suggest these limitations.

As previously described, Carr must be considered in its entirety, including disclosures that teach away from the claims. Further, the Examiner cannot argue that distribution inherently teaches the claimed invention without providing rationale or evidence tending to show inherency. Neither the text nor the distribution algorithm of Carr teaches or suggests "the detail loops cause storage of the vector memory references in temporary arrays that are allocated consecutively so that no temporary arrays elements are cache synonyms" as required in claim 17. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 17 and all claims that depend from claim 17 are allowable.

D. Claim 24

Amended claim 24, in part, requires "distributing the vector memory references into a plurality of detail loops configured to retrieve strips of the vector memory references and store the strips in temporary arrays." Carr does not teach or suggest this limitation.

As previously described, Carr must be considered in its entirety, including disclosures that teach away from the claims. Further, the Examiner cannot argue that distribution inherently teaches the claimed invention without providing

rationale or evidence tending to show inherency. Neither the text nor the distribution algorithm of Carr teaches or suggests "detail loops configured to retrieve strips of the vector memory references and store the strips in temporary arrays" as required in claim 24. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 24 and all claims that depend from claim 24 are allowable.

E. Claim 25

Amended claim 25, in part, requires "distributing the vector memory references into a plurality of detail loops configured to allocate the vector memory references into temporary arrays that avoid cache synonyms." Carr does not teach or suggest this limitation.

As previously described, Carr must be considered in its entirety, including disclosures that teach away from the claims. Further, the Examiner cannot argue that distribution inherently teaches the claimed invention without providing rationale or evidence tending to show inherency. Neither the text nor the distribution algorithm of Carr teaches or suggests "detail loops configured to allocate the vector memory references into temporary arrays that avoid cache synonyms" as required in claim 25. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 25 is allowable.

F. Claim 26

Amended claim 26, in part, requires "distributing the vector memory references into a plurality of detail loops configured to serially process strips of the vector memory references so that thrashing does not occur." Carr does not teach or suggest this limitation.

As previously described, Carr must be considered in its entirety, including disclosures that teach away from the claims. Further, the Examiner cannot argue that distribution inherently teaches the claimed invention without providing rationale or evidence tending to show inherency. Neither the text nor the distribution algorithm of Carr teaches or suggests "detail loops configured to

serially process strips of the vector memory references so that thrashing does not occur" as required in claim 26. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 26 and all claims that depend from claim 26 are allowable.

G. Claim 33

Amended claim 33, in part, requires "distributing cache synonyms into detail loops configured to allocate the cache synonyms into temporary storage areas, sized and located, to prevent cache thrashing." Carr does not teach or suggest this limitation.

As previously described, Carr must be considered in its entirety, including disclosures that teach away from the claims. Further, the Examiner cannot argue that distribution inherently teaches the claimed invention without providing rationale or evidence tending to show inherency. Neither the text nor the distribution algorithm of Carr teaches or suggests "detail loops configured to allocate the cache synonyms into temporary storage areas, sized and located, to prevent cache thrashing" as required in claim 33. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 33 and all claims that depend from claim 33 are allowable.

H. Claim 35

Amended claim 35, in part, requires "reducing cache thrashing by distributing the portion of the memory references into distinct loops that allocate strips of the memory references into temporary arrays for execution." Carr does not teach or suggest this limitation.

As previously described, Carr must be considered in its entirety, including disclosures that teach away from the claims. Further, the Examiner cannot argue that distribution inherently teaches the claimed invention without providing rationale or evidence tending to show inherency. Neither the text nor the distribution algorithm of Carr teaches or suggests "distributing the portion of the memory references into distinct loops that allocate strips of the memory references into temporary arrays for execution" as required in claim 35. None of

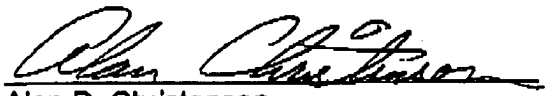
the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations. For at least these reasons, Applicants submit that claim 35 is allowable.

II. CONCLUSIONS

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



Alan D. Christenson
PTO Reg. No. 54,036
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
AGENT FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400